Forward Conduction Instability of Quasi-Vertical GaN p-i-n Diodes on Si Substrates

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***Abstract*— This article reports trap-related forward conduction instability of GaN quasi-vertical p-i-n diodes grown on a Si substrate. Three hole traps with activation energies of 0.38, 0.60, and 0.70 eV together with one electron trap with an energy level of 0.26 eV under the conduction band were revealed by deep-level transient spectroscopy (DLTS). Pulsed *I–V* measurements were performed on a device whose traps were prefilled. The rest time durations and OFF-state bias levels and periods were varied to investigate the forward *I–V* recovery phenomenon, which was highly correlated with the carrier detrapping process inside the device. The detrapping process could be greatly accelerated by a reverse bias or a lifted temperature. An "on-the-fly" resistance characterization was carried out to study the time-dependent carrier release process using short positive voltage pulses. The device was further submitted to switch-on transient assessment to investigate the time-resolved dynamic R_{ON} evolution. The initial dynamic R_{ON} ratio was proportional to the reverse bias level and duration and was gradually decreased after continuous carrier injection until the trapping effects were overwhelmed. With a forward voltage slightly higher than the threshold voltage, it took dozens of milliseconds for the dynamic R_{ON} to be equal to its static counterpart. It was found that at 350 K, the ON-resistance ratio could reach unit more rapidly than the room temperature case, indicating mitigation of current collapse of p-i-n diodes and their great potential for high-temperature switching applications.**

***Index Terms*— Conduction instability, deep-level transient spectroscopy (DLTS) measurement, dynamic R_{ON}, GaN quasi-vertical p-i-n diodes, pulsed measurements, trap effects.**

I. Introduction

WURTZITE GaN semiconductors have attracted considerable research interest for next-generation optoelectronic [1], [2] and electronic devices [3]–[5], due to their large energy bandgap, high critical electrical field, and high electron mobility [6], [7]. For example, AlGaN/GaN-based HEMTs have been regarded as a promising candidate for high-power high-frequency switching applications. In the past decade, there have also been extensive research efforts in the development of GaN p-i-n diodes which feature high breakdown voltage with a small device footprint, outstanding forward conduction capability, and low reverse leakage current [8]–[16].

So far, GaN-based p-i-n diodes have been successfully reported for a variety of substrates, including GaN [8], [10], [14]–[16], SiC [17], sapphire [18], [19], and Si substrates [9], [11]–[13], [20]. GaN p-i-n diodes with excellent breakdown voltage of up to several kilovolts have been demonstrated using a thick drift layer [15]. Recently, a steady progress has been reported for GaN p-i-n diodes grown on Si substrates as the improvement of material growth techniques, particularly the capability of growing thick GaN epitaxial layers on Si substrates. With a 4-μm-thick drift layer, a breakdown voltage of 823 V has been demonstrated using GaN-on-Si epitaxial layers [9]. Repeated breakdown capability has also been reported for GaN p-i-n diodes on Si, suggesting their high reliability and great potential for protection applications [21].

However, previous studies on GaN p-i-n diodes mostly focused on reporting the steady-state performance of GaN p-i-n diodes, while a systematic investigation of the dynamic performance of GaN p-i-n diode is still missing. The dynamic stability issue induced by carrier trapping/detrapping process may lead to threshold voltage instability, dynamic ON-resistance degradation, and so on. The dynamic stability including current collapse phenomenon has been extensively researched for GaN metal–insulator–semiconductor (MIS) HEMT and could be a practical issue for real use of GaN devices [22]–[34]. Different from the dynamic study of (MIS) HEMT which was typically associated with the trapping effects at the device surface, along the interface of AlGaN and dielectric layer, or about electron injection from the substrate [22], [24], [32]–[36], the study of GaN p-i-n diode dynamic performance opened a path for directly pinpointing the trap effects inside the GaN drift layer.

In this study, pulsed *I–V* measurements and deep-level transient spectroscopy (DLTS) were performed on GaN p-i-n diodes grown and fabricated on Si substrates. The impact of idle time duration, reverse bias stress level, and period on device forward conduction capability was quantitatively investigated. Three hole trap levels and one electron trap level were extracted from the capacitance-transient-based DLTS

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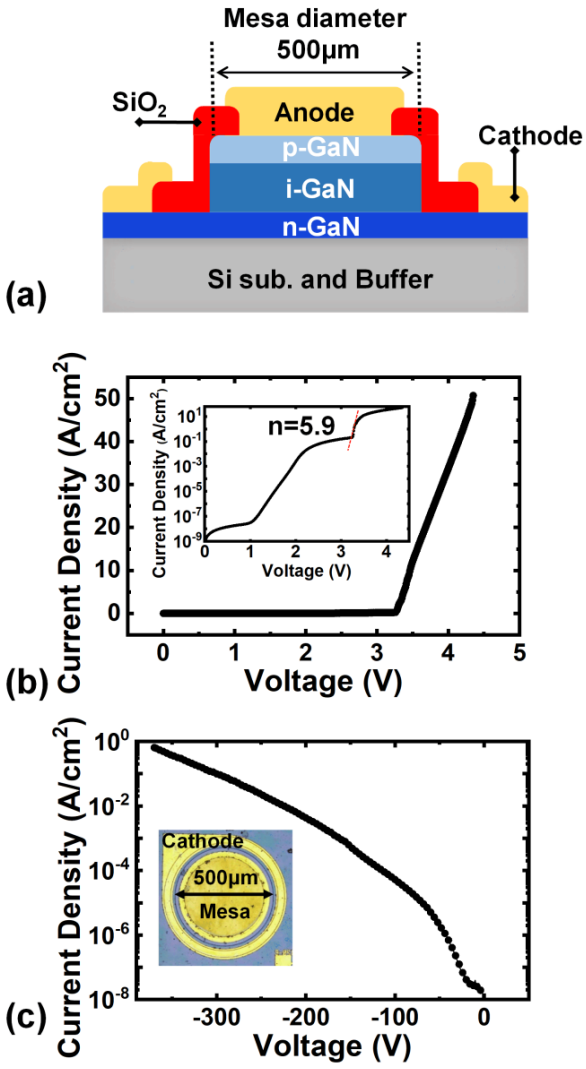

Fig. 1. (a) Schematic cross section of GaN-on-Si quasi-vertical p-i-n diodes. (b) Forward and (c) reverse *I–V* characteristics of quasi-vertical p-i-n diodes. Inset: an optical image of device under test with a mesa diameter of 500 μm.

measurements. The measurement methods reported here could also be useful for direct identification of traps in GaN layers on Si without involvement of conductive substrate or dielectric layers.

II. Experimental

The sample used in this study was a GaN-based quasi-vertical p-i-n diode grown on a Si substrate by metal–organic chemical vapor deposition (MOCVD) phase epitaxy. Fig. 1(a) illustrates a schematic cross section of a fabricated p-i-n structure on Si which starts from a 1.6-μm-thick graded AlGaN and GaN buffer, followed by a 500-nm-thick Si-doped n-GaN layer (electron concentration $n = 1 \times 10^{19}$ cm^{-3}), a 2-μm-thick undoped i-GaN layer (carrier concentration on the order of 10^{16} cm^{-3}), and a 500-nm-thick Mg-doped p-GaN layer (hole concentration $p = 2 \times 10^{17}$ cm^{-3} at 300 K). The device fabrication process began with mesa etching to expose the n-GaN layer using Cl_2-based inductively coupled

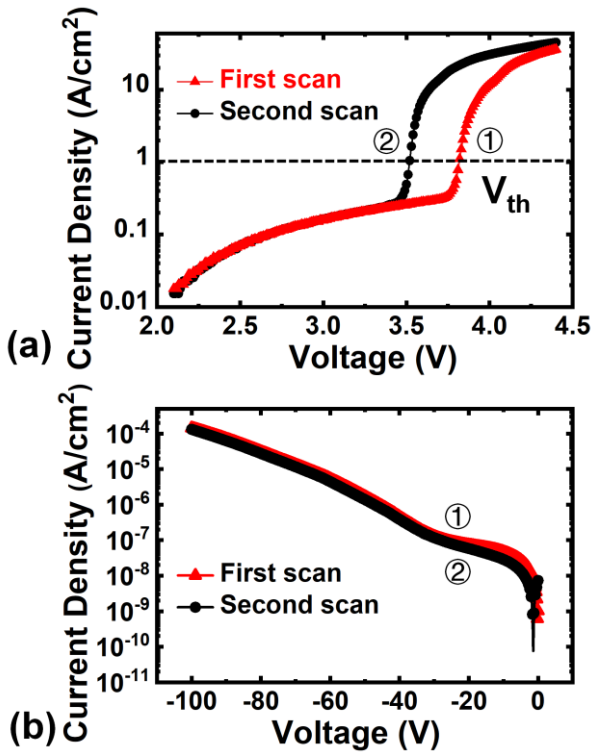

Fig. 2. (a) Forward and (b) reverse *I–V* characteristics of GaN-on-Si quasi-vertical p-i-n diodes by the first scan and a follow-up second scan.

plasma (ICP) etching. A Ni/Au stack was deposited and annealed to form ohmic contacts to the p-GaN. Subsequently, a SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) for device sidewall passivation and the quasi-vertical device was finished by depositing Cr/Al-based metal as electrodes.

DLTS measurements were directly performed on the diodes on wafer from 150 to 350 K. Pulsed $I–V$ measurements were applied onto the device with various rest time durations, OFF-state bias levels, and periods to investigate the carrier detrapping process, in addition to "on-the-fly" resistance characterization. The device was further submitted to switch-on transient assessment to investigate the role of trapping process on dynamic R_{ON}. The above experiments were also implemented at 350 K to discuss the forward conduction instability at a relatively higher temperature.

III. Results and Discussion

Fig. 1(b) shows the forward current–voltage ($I-V$) characteristics of the p-i-n device (mesa diameter = 500 μm) in linear and log scales. Using the 1-A/cm^2 standard, a typical turn-on voltage was determined to be 3.3 V under dc condition and an ideality factor n of 5.9 was extracted. Before the turn-on voltage, a current ledge was observed due to relatively short injected carrier lifetime, thus short diffusion length and insufficient number of carriers stored in the drift layer, leading to a gradual slope of the $J–V$ graph. Beyond the turn-on voltage, the forward current density was increased rapidly due to the carrier injection into the drift layer, where conductivity modulation was observed. When reverse biased, the leakage

current was only -2×10^{-3} A/cm^2 at -200 V. With a 2-μm-thick undoped i-GaN layer, the quasi-vertical p-i-n rectifier demonstrated a breakdown voltage (V_{br}) of about 380 V [see Fig. 1(c)] using -1 A/cm^2 as the breakdown criteria. It is noted that the 500-μm device had nearly identical leakage current density and breakdown voltage as those with smaller dimensions, indicating uniform GaN crystalline quality and leakage current originating from GaN thin film rather than the sidewall surfaces [37].

Fig. 2(a) shows the forward characteristics of the GaN p-i-n diodes upon two consecutive pulsed I–V sweep scans. The first scan (from 0 to 4.5 V) was performed for a device which had been rested for several hours; next, a follow-up second scan was conducted on the same device. One may find the threshold voltage was negatively shifted from 3.82 V in the first scan to 3.52 V in the second scan.

Starting from the second scan, the consecutive I–V curves were typically overlaid with each other. However, if the device was rested for a sufficiently long time, for example, several minutes, the I–V curve would be reversed to the one labeled as the first scan in Fig. 2(a). The phenomenon suggested a carrier trapping/detrapping process that the traps were filled in as the injection of carriers (forward bias in the first scan), whereas it took some time to detrap the carriers. Thus, in the second scan, the injected carriers did not have to fill the traps before they can contribute to the conduction that a smaller threshold voltage was observed, compared with the virgin device status. Fig. 2(b) shows that the reverse I–V characteristics were kept unchanged for consecutive scans, with a leakage current density of 10^{-4} A/cm^2 at a reverse bias of -100 V.

The forward conduction curve shift suggested interaction between traps and injected carriers (both electrons and holes) inside the diode, so the p-i-n diode was sent for capacitance-transient-based DLTS measurements from 150 to 350 K. A representative DLTS spectrum recorded for a 500-μm-sample is displayed in Fig. 3(a). The DLTS signals [38], [39] revealed one majority carrier trap (electron trap) labeled as E_1 with an activation energy of 0.26 eV at 200 K, and three minority carrier traps (hole traps) labeled as H_1, H_2, and H_3 with an activation energy of 0.38, 0.60, and 0.70 eV at 230, 310, and 340 K, respectively, [see Fig. 3(b)]. Table I summarized the detailed information of four traps mentioned above. A separate capacitance-transient-based measurement indicated that the space charge region width was slightly larger than 2 μm, suggesting that the electrically active traps were mainly distributed in the 2-μm-thick drift layer. The extracted trap properties indicated that both the electrons and the holes could be captured simultaneously at forward conduction. The origin of traps was probably related to the nitrogen vacancies existed in the GaN-on-Si epitaxial layer [40], [41].

To investigate the overall influence of the carrier detrapping process on forward conduction capability of the GaN p-i-n diode, multiple consecutives pulsed I–V measurements with various "rest time" durations in between were carried out, as summarized in Fig. 4. In this experiment, the device was preforward biased to inject carriers to the traps that the initial state refers to a "filled" trap state. As shown in Fig. 4(a),

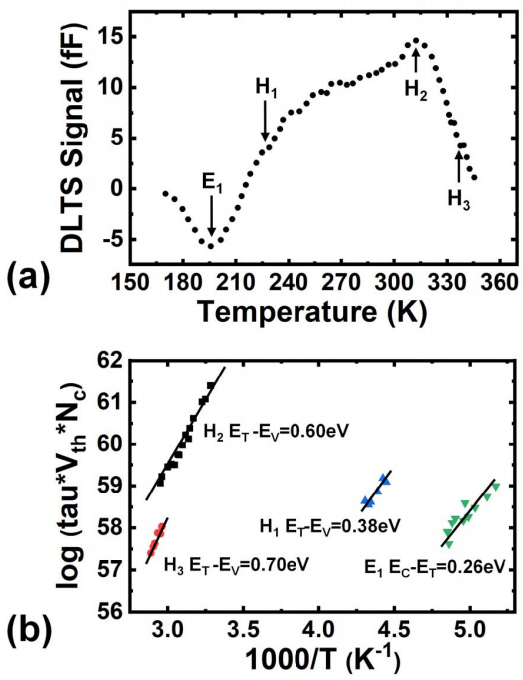

Fig. 3. (a) Typical capacitance-based DLTS spectrum for GaN-on-Si quasi-vertical p-i-n diodes with the following parameters: $V_p = 1.2$ V, $V_r = -3$ V, and $t_p = 100$ ms, where V_p is the pulse voltage, V_r is the reverse bias voltage, and t_p is the pulsewidth. (b) Arrhenius plot of log(tau$*V_{th}*N_c$) versus 1000/T for obtained majority and minority carrier traps of GaN-on-Si quasi-vertical p-i-n diode.

TABLE I
ENERGY LEVELS, CAPTURE CROSS SECTION, AND TRAP CONCENTRATION FOR THE DEVICE UNDER TEST

Trap No.	Energy Level (eV)	Capture Cross section (cm^2)	Trap Concentration N_T (cm^{-3})
E_1	E_c-0.26	2.59×10^{-19}	9.37×10^{14}
H_1	E_v+0.38	7.16×10^{-18}	7.68×10^{15}
H_2	E_v+0.60	2.18×10^{-17}	1.94×10^{15}
H_3	E_v+0.70	1.60×10^{-15}	3.72×10^{15}

pulse-based I–V measurements were performed after a certain amount of rest time from 2 to 25 s. The pulse voltage for each measurement was set to increase from 0 to 4.5 V, with pulsewidth and period of 1 and 5 ms, to minimize the thermal influence.

In Fig. 4(b), it was found that with a 2-s rest time, the forward I–V was positively shifted by 0.2 V, suggesting the occurrence of carrier release from trapped states inside the drift layer due to thermal emission. As the rest time was extended, the threshold voltage was further positively shifted continuously. When the rest time was set as 25 s, a nearly complete natural recovery of I–V characteristic was achieved, indicating that the detrapping process may take dozens of seconds to finish.

In addition to the study on zero-volt rest time duration effects, the influence of reverse bias on the recovery of forward I–V characteristics to achieve fresh unfilled state has also been studied [see Fig. 5(a)]. Again, the device was prebiased to inject carriers to the traps that the initial state refers to a

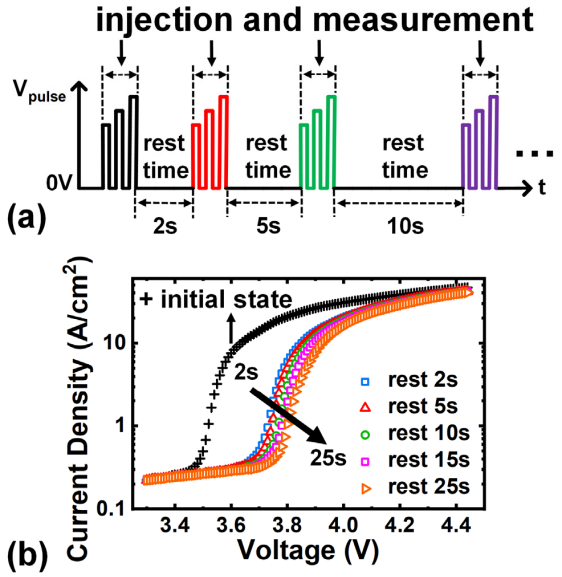

Fig. 4. (a) Schematic pulsed *I–V* measurement waveforms with various rest time durations between each measurement session. (b) Forward *I–V* characteristics at 300 K with various rest time durations.

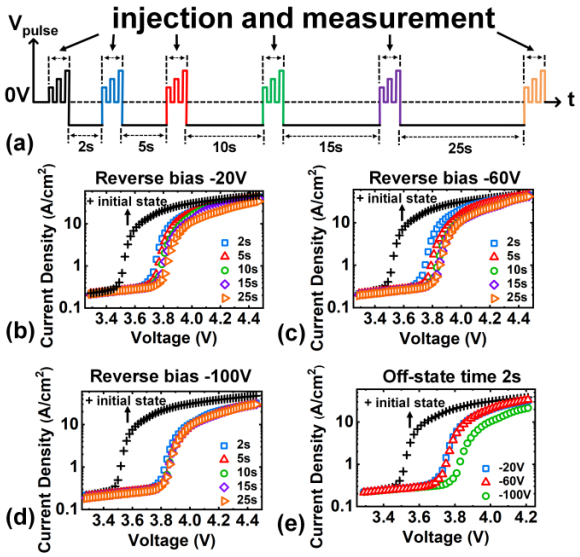

Fig. 5. (a) Schematic waveforms used in reverse bias/time-dependent measurements. (b)–(d) Forward bias *I–V* characteristics at 300 K upon application of −20, −60, and −100 V quiescent base voltage for various time; the initial state refers to a "filled" trap state. (e) Forward bias *I–V* characteristics upon applied reverse bias of −20, −60, and −100 V while keeping OFF-state time 2 s.

"filled" trap state. As shown in Fig. 5(b)–(d), as the reverse bias applied on the device after each injection period was increased, the time it took for the p-i-n diode to complete the recovery process to a fresh state was shortened. It suggested that the carrier detrapping process could be accelerated as the OFF-state bias level was enhanced.

The phenomenon is also illustrated in Fig. 5(e) that given a fixed 2-s OFF-state duration, a reverse bias of −100 V resulted in a further threshold voltage shift than the cases of −20 and −60 V. In addition to a further positively shifted threshold voltage, the forward current density of the "−100 V case" in

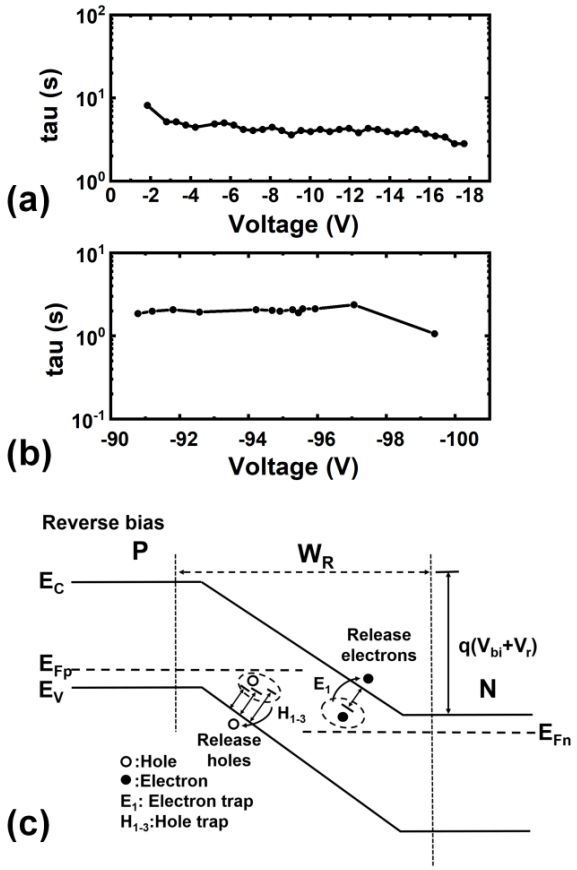

Fig. 6. Voltage dependence of carrier emission time constants at 300 K, obtained using the isothermal DLTS analysis mode with variable reverse bias at (a) small reverse bias range from 0 to −20 V and (b) large bias range from −90 to −100 V. (c) Schematic of the nonequilibrium energy band diagram under reverse bias and related detrapping process mechanism.

the high-level injection region was also slightly lower than the other two cases, also indicating greater extent of trap depletion assisted by the electrical field [42].

The electrical-field-dependent carrier release time constant was also extracted by the capacitance-transient-based measurements, as shown in Fig. 6. It was found that the time constant at relatively low reverse bias, namely, under −20 V, was 4.0 s ± 0.5 s [see Fig. 6(a)]. This agrees well with Fig. 5(b) that the recovery process under low reverse bias was typically the same as those without reverse bias [Fig. 4(b)].

The carrier detrapping time constant dropped with the increase in the reverse bias. When V_R was in the range of −90 to −100 V, the time constant was measured to be 2.0 s ± 0.3 s, which matched well with the phenomenon shown in Fig. 5(d) and (e).

Fig. 6(c) shows the nonequilibrium energy band diagram under reverse bias, with three hole traps H_1 (0.38 eV), H_2 (0.60 eV), and H_3 (0.70 eV) and one electron trap E_1 (0.26 eV) illustrated. In the reverse bias condition, E_{Fn} and E_{Fp} were separated from their equilibrium states that the electrons and holes' release process become a dominating mechanism. Once the traps were depleted, when the diode was forward biased, a portion of injected carriers have to fill the traps before contributing to the conductive current.

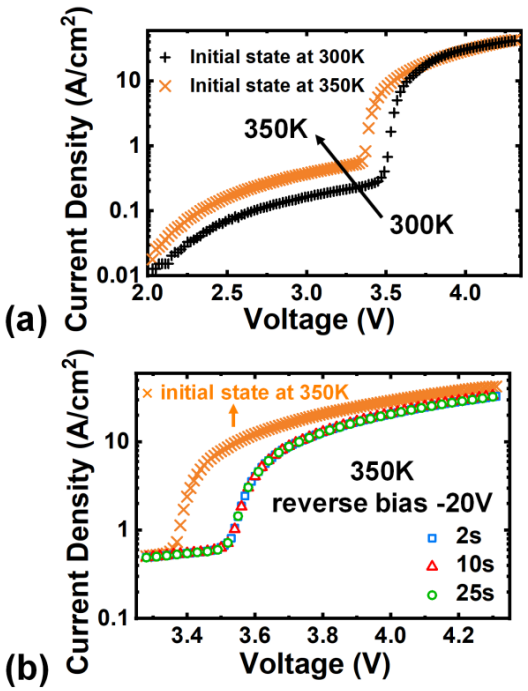

Fig. 7. (a) Comparison of the initial states at 350 and 300 K. (b) Forward bias *I*–*V* characteristics upon applied reverse bias of −20 V quiescent base voltage for various time at 350 K.

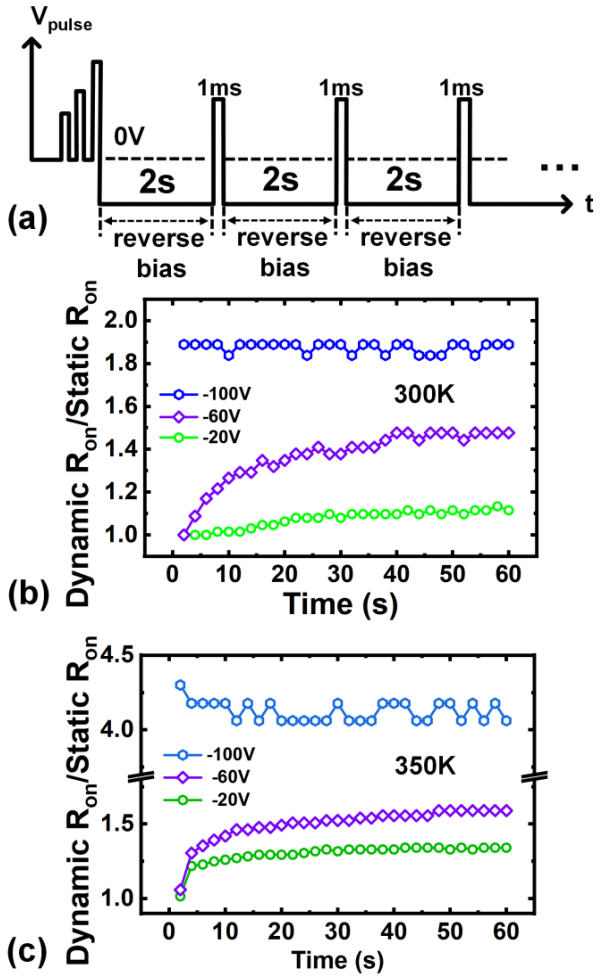

Fig. 8. (a) Schematic waveforms of "on-the-fly" ON-resistance measurement. (b) and (c) Dependence of dynamic R_{ON}/static R_{ON} on reverse bias duration with various reverse voltages at 300 and 350 K, respectively.

The forward conduction at a lifted temperature is shown in Fig. 7. Fig. 7(a) shows a comparison of the initial states at 350 and 300 K. At 350 K, the diffusion current ledge level was slightly higher than the one at 300 K due to higher intrinsic background carrier density inside the drift layer. Also, the threshold voltage was 0.14 V lower than that at 300 K. As shown in Fig. 7(b), at 350 K, only 0.15 V threshold voltage shift was observed with a reverse bias of −20 V, and full recovery could be achieved within 2 s. This phenomenon demonstrated that higher temperature would accelerate the detrapping process of the captured electrons and holes.

To further investigate the electrical field and temperature-assisted detrapping process, an "on-the-fly" ON-resistance measurement was performed, as shown in Fig. 8. In this measurement, the device was subject to the reverse stressing conditions in a quasi-continuous manner that a short 3-V positive-bias pulse (pulsewidth = 1 ms) was periodically applied to switch the diode on and pin-point the ON-resistance at that moment. Thus, a time-resolved dynamic ON-resistance graph can be revealed. With a reverse bias of −20 V at room temperature, the dynamic R_{ON}/static R_{ON} ratio extracted at a forward voltage of 3 V was increased to 1.1 after 30 s stressing. As the reverse stress voltage was increased, the time that the ON-resistance ratio got saturated was shortened and a larger ON-resistance ratio was observed. For the −100 V case, the ratio hit 1.9 from the beginning of the measurement time span. This could be understood as that deep-level traps can only be depleted to release carriers by large electrical field and/or long stressing time, and thus more severe current degradation was observed [36]. At 350 K, the ON-resistance ratio was further degraded for all the reverse bias steps, indicating a greater extent of trap depletion and a shorter carrier emission time constant at a higher temperature of 350 K.

Fig. 9 presents the transient performance of GaN p-i-n diode when being switched on after exposure to large OFF-state bias to investigate the carrier trapping process. The current-time dependence was recorded and the dynamic R_{ON} was normalized with respect to the static R_{ON} extracted from the *I*–*t* sampling test in which the traps were already filled. As the forward bias was as low as 3 V, the initial dynamic R_{ON}/static R_{ON} ratio was found to be increased with the increase in the reverse bias duration, and reverse bias level, as shown in Fig. 9(a) and (b), respectively. With increased reverse bias level from −20 to −100 V, the initial dynamic R_{ON} ratio went from 1.07 to 1.57, indicating that larger portion of the trap states have been emptied with higher electrical field applied, which was in good agreement with the observation in Fig. 5. In all the cases, the dynamic R_{ON} was gradually decreased as the forward bias was continuously applied on the device. As the injection level was quite low due to small forward bias of 3 V, the ratio could not reach unit even when the measurement time scale was set as 200 ms.

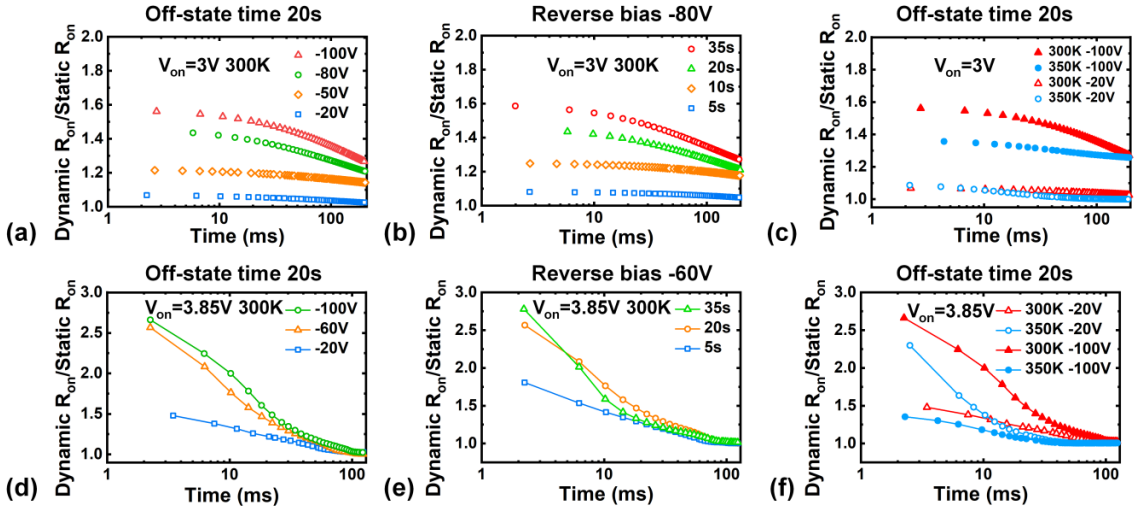

Fig. 9. (a) and (d) Time-resolved dynamic R_{ON}/static R_{ON} at 300 K with reverse bias varying from −20 to −100 V at 3 and 3.85 V positive bias, respectively. (b) and (e) Time-resolved dynamic R_{ON}/static R_{ON} at 300 K with OFF-state time varying from 5 to 35 s at 3 and 3.85 V positive bias, respectively. (c) and (f) Time-resolved dynamic R_{ON}/static R_{ON} at 300 and 350 K.

The same measurements were also implemented using a relatively larger forward bias of 3.85 V (slightly higher than the threshold voltage). As shown in Fig. 9(e), with a reverse bias of −60 V for a period of 5–35 s, an initial dynamic R_{ON} ratio of 1.8–2.8 was observed and quickly reduced to unit after 100 ms injection at 3.85 V, indicating that the E-field-induced depleted trap states could be quickly filled upon numerous carrier injection using a voltage beyond the threshold voltage. Moreover, the switch-on experiment was repeated at 350 K, as summarized in Fig. 9(f). With a reverse bias of −100 V applied on the diode for 20 s, it took 6 ms to drop the ON-resistance ratio to 1.2 and 40 ms to reach unit. Overall, the dropping of ratio was much speeded up at 350 K, compared with the results at 300 K, indicating promotion of the carrier trapping process at a high temperature as well, in addition to the acceleration of the carrier release process at 350 K, as demonstrated in Fig. 8(c). These findings proved that p-i-n diodes on Si held limited current collapse upon off–on switch at 350 K, showing their great potential for high-temperature high-voltage switching applications.

IV. Conclusion

In summary, the forward conduction instability and the dynamic ON-resistance performance of GaN-on-Si quasi-vertical p-i-n diodes have been evaluated using pulsed I–V methods and DLTS. It was found that the traps inside the GaN diode captured carriers during the injection process and released carriers w/wo reverse bias, resulting in current density degradation and threshold voltage instability. From the DLTS analyses, one electron trap at 0.26 eV below the conduction band and three hole trap levels at 0.38, 0.60, and 0.70 eV above the valance band were observed, indicating that both the electrons and holes were responsible for the conduction instability. Larger reverse bias and/or longer OFF-state time could promote drop of forward conductivity. Both the pulsed I–V measurements and DLTS capacitance transient results indicated that the detrapping time constant was about 4 s under −20 V and 2 s at a voltage of −100 V. Time-dependent "on-the-fly" ON-resistance sampling test without perturbing the device reverse biased state was implemented to investigate the electrical field and temperature-assisted detrapping process. Diode transient performance was studied using two different positive bias voltages. At 3.85 V, it took nearly 100 and 40 ms to recover the dynamic ON-resistance to be equal to its static counterpart at 300 and 350 K, respectively. At a higher temperature, both the trapping and detrapping processes are accelerated. The characteristics obtained in this article provide an understanding of the trapping/detrapping process in the GaN p-i-n diodes on Si and show that the current collapse of the p-i-n diode could be mitigated at 350 K, suggesting the great potential of p-i-n diodes for high-temperature switching applications.

References

[1] G. Li *et al.*, "GaN-based light-emitting diodes on various substrates: A critical review," *Rep. Prog. Phys.*, vol. 79, no. 5, p. 45, May 2016, doi: 10.1088/0034-4885/79/5/056501.

[2] T. D. Moustakas and R. Paiella, "Optoelectronic device physics and technology of nitride semiconductors from the UV to the terahertz," *Rep. Prog. Phys.*, vol. 80, no. 10, p. 41, Oct. 2017, doi: 10.1088/1361-6633/aa7bb2.

[3] K. J. Chen *et al.*, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[4] H. Amano *et al.*, "The 2018 GaN power electronics roadmap," *J. Phys. D, Appl. Phys.*, vol. 51, no. 16, p. 48, Apr. 2018, doi: 10.1088/1361-6463/aaaf9d.

[5] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[6] M. Kuzuhara, J. T. Asubar, and H. Tokuda, "AlGaN/GaN high-electron-mobility transistor technology for high-voltage and low-on-resistance operation," *Jpn. J. Appl. Phys.*, vol. 55, no. 7, p. 12, Jul. 2016, doi: 10.7567/jjap.55.070101.

[7] I. Rossetto *et al.*, "Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2334–2339, Jun. 2016, doi: 10.1109/TED.2016.2553721.

[8] C.-W. Tsou, M.-H. Ji, M. Bakhtiary-Noodeh, T. Detchprohm, R. D. Dupuis, and S.-C. Shen, "Temperature-dependent leakage current characteristics of homojunction GaN p-i-n rectifiers using ion-implantation isolation," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4273–4278, Oct. 2019, doi: 10.1109/TED.2019.2933421.

[9] R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, "820-V GaN-on-Si quasi-vertical p-i-n diodes with BFOM of 2.0 GW/cm^2," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 401–404, Mar. 2018, doi: 10.1109/LED.2018.2793669.

[10] H. Fu *et al.*, "High performance vertical GaN-on-GaN p-n power diodes with hydrogen-plasma-based edge termination," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1018–1021, Jul. 2018, doi: 10.1109/LED.2018.2837625.

[11] Y. Zhang *et al.*, "High-performance 500 V quasi- and fully-vertical GaN-on-Si pn diodes," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 248–251, Feb. 2017, doi: 10.1109/LED.2016.2646669.

[12] X. Zhang, X. Zou, X. Lu, C. W. Tang, and K. M. Lau, "Fully- and quasi-vertical GaN-on-Si p-i-n diodes: High performance and comprehensive comparison," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 809–815, Mar. 2017, doi: 10.1109/TED.2017.2647990.

[13] X. Zou, X. Zhang, X. Lu, C. W. Tang, and K. M. Lau, "Fully vertical GaN p-i-n diodes using GaN-on-Si epilayers," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 636–639, May 2016, doi: 10.1109/LED.2016.2548488.

[14] K. Nomoto *et al.*, "1.7-kV and 0.55-m$\Omega\cdot$cm^2 GaN p-n diodes on bulk GaN substrates with avalanche capability," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 161–164, Feb. 2016, doi: 10.1109/LED.2015.2506638.

[15] H. Ohta *et al.*, "Vertical GaN p-n junction diodes with high breakdown voltages over 4 kV," *IEEE Electron Device Lett.*, vol. 36, no. 11, pp. 1180–1182, Nov. 2015, doi: 10.1109/LED.2015.2478907.

[16] Z. Hu *et al.*, "1.1-kV vertical GaN p-n diodes with p-GaN regrown by molecular beam epitaxy," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1071–1074, Aug. 2017, doi: 10.1109/LED.2017.2720747.

[17] J. B. Limb, D. Yoo, J.-H. Ryou, S. C. Shen, and R. D. Dupuis, "Low on-resistance GaN pin rectifiers grown on 6H-SiC substrates," *Electron. Lett.*, vol. 43, no. 6, pp. 67–68, Mar. 2007, doi: 10.1049/el:20070065.

[18] J. Howell-Clark *et al.*, "Improved electrical performance of MOCVD-grown GaN p-i-n diodes with high-low junction p-layers," *Solid-State Electron.*, vol. 162, Dec. 2019, Art. no. 107646, doi: 10.1016/j.sse.2019.107646.

[19] Z. Zhu *et al.*, "Effects of 10 MeV electron irradiation on the characteristics of gallium-nitride-based pin alpha-particle detectors," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 902, pp. 9–13, Sep. 2018, doi: 10.1016/j.nima.2018.06.040.

[20] S. Mase, Y. Urayama, T. Hamada, J. J. Freedsman, and T. Egawa, "Novel fully vertical GaN p-n diode on Si substrate grown by metalorganic chemical vapor deposition," *Appl. Phys. Express*, vol. 9, no. 11, Nov. 2016, Art. no. 111005, doi: 10.7567/apex.9.111005.

[21] X. Zou, X. Zhang, X. Lu, C. W. Tang, and K. M. Lau, "Breakdown ruggedness of quasi-vertical GaN-based p-i-n diodes on Si substrates," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1158–1161, Sep. 2016, doi: 10.1109/LED.2016.2594821.

[22] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng, and K. J. Chen, "Impact of substrate bias polarity on buffer-related current collapse in AlGaN/GaN-on-Si power devices," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 5048–5056, Dec. 2017, doi: 10.1109/TED.2017.2764527.

[23] S. Yang, S. Han, K. Sheng, and K. J. Chen, "Dynamic on-resistance in GaN power devices: Mechanisms, characterizations, and modeling," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1425–1439, Sep. 2019, doi: 10.1109/JESTPE.2019.2925117.

[24] M. Meneghini *et al.*, "Temperature-dependent dynamic R_{ON} in GaN-based MIS-HEMTs: Role of surface traps and buffer leakage," *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 782–787, Mar. 2015, doi: 10.1109/TED.2014.2386391.

[25] A. N. Tallarico *et al.*, "PBTI in GaN-HEMTs with p-type gate: Role of the aluminum content on ΔV_{TH} and underlying degradation mechanisms," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 38–44, Jan. 2018, doi: 10.1109/ted.2017.2769167.

[26] J. B. He, G. F. Tang, and K. J. Chen, "V_{TH} instability of p-GaN gate HEMTs under static and dynamic gate stress," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1576–1579, Oct. 2018, doi: 10.1109/LED.2018.2867938.

[27] J. Wei *et al.*, "Charge storage mechanism of drain induced dynamic threshold voltage shift in p-GaN gate HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 526–529, Apr. 2019, doi: 10.1109/LED.2019.2900154.

[28] T. Cappello, A. Santarelli, and C. Florian, "Dynamic R_{ON} characterization technique for the evaluation of thermal and off-state voltage stress of GaN switches," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3386–3398, Apr. 2018, doi: 10.1109/TPEL.2017.2710281.

[29] X. Tang, B. Li, Z. Zhang, G. Tang, J. Wei, and K. J. Chen, "Characterization of static and dynamic behaviors in AlGaN/GaN-on-Si power transistors with photonic-ohmic drain," *IEEE Trans. Electron Devices*, vol. 63, no. 7, pp. 2831–2837, Jul. 2016, doi: 10.1109/TED.2016.2567442.

[30] S. Yang, Y. Y. Lu, H. X. Wang, S. H. Liu, C. Liu, and K. J. Chen, "Dynamic gate stress-induced V_{TH} shift and its impact on dynamic R_{ON} in GaN MIS-HEMTs," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 157–160, Feb. 2016, doi: 10.1109/LED.2015.2505334.

[31] N. Badawi, O. Hilt, E. Bahat-Treidel, J. Bocker, J. Wurfl, and S. Dieckerhoff, "Investigation of the dynamic on-state resistance of 600 V normally-off and normally-on GaN HEMTs," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4955–4964, Nov. 2016, doi: 10.1109/TIA.2016.2585564.

[32] M. Meneghini *et al.*, "Buffer traps in fe-doped AlGaN/GaN HEMTs: Investigation of the physical properties based on pulsed and transient measurements," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4070–4077, Dec. 2014, doi: 10.1109/TED.2014.2364855.

[33] D. Bisi *et al.*, "Deep-level characterization in GaN HEMTs—Part I: Advantages and limitations of drain current transient measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct. 2013, doi: 10.1109/TED.2013.2279021.

[34] A. Chini, F. Soci, M. Meneghini, G. Meneghesso, and E. Zanoni, "Deep levels characterization in GaN HEMTs—Part II: Experimental and numerical evaluation of self-heating effects on the extraction of traps activation energy," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3176–3182, Oct. 2013, doi: 10.1109/TED.2013.2278290.

[35] J. Hu *et al.*, "Current transient spectroscopy for trapping analysis on Au-free AlGaN/GaN Schottky barrier diode," *Appl. Phys. Lett.*, vol. 106, no. 8, Feb. 2015, Art. no. 083502, doi: 10.1063/1.4913575.

[36] J. Hu *et al.*, "Physical origin of current collapse in Au-free AlGaN/GaN Schottky barrier diodes," *Microelectron. Rel.*, vol. 54, nos. 9–10, pp. 2196–2199, Sep. 2014, doi: 10.1016/j.microrel.2014.07.031.

[37] Y. Zhang *et al.*, "Design space and origin of off-state leakage in GaN vertical power diodes," presented at the IEDM Tech. Dig., Dec. 2015, doi: 10.1109/IEDM.2015.7409830.

[38] W. Sun *et al.*, "Investigation of trap-induced threshold voltage instability in GaN-on-Si MISHEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 890–895, Feb. 2019, doi: 10.1109/TED.2018.2888840.

[39] W. Zhang, E. Simoen, M. Zhao, and J. Zhang, "Analysis of leakage mechanisms in AlN nucleation layers on p-Si and p-SOI substrates," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1849–1855, Apr. 2019, doi: 10.1109/TED.2019.2899964.

[40] W.-J. Wang, C.-L. Liao, Y.-F. Chang, Y.-L. Lee, C.-L. Ho, and M.-C. Wu, "DLTS analyses of GaN p-i-n diodes grown on conventional and patterned sapphire substrates," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1376–1378, Nov. 2013, doi: 10.1109/LED.2013.2281456.

[41] L.-W. Shan, Z.-Y. Liu, M.-P. Lin, C.-J. Yu, K.-C. Hsieh, and M.-C. Wu, "Electrical analyses of GaN PIN diodes grown on patterned sapphire substrates," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron., Mater., Process., Meas., Phenomena*, vol. 35, no. 5, Sep. 2017, Art. no. 052203, doi: 10.1116/1.4997900.

[42] C. Sharma, R. Laishram, Amit, D. S. Rawal, S. Vinayak, and R. Singh, "Investigation on de-trapping mechanisms related to non-monotonic kink pattern in GaN HEMT devices," *AIP Adv.*, vol. 7, no. 8, Aug. 2017, Art. no. 085209, doi: 10.1063/1.4985057.